UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,303	09/04/2003	Hoe-Ju Chung	9898-293	8209

20575 7590 11/17/2004

MARGER JOHNSON & MCCOLLOM PC
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,303	CHUNG ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwak (U.S. pat. No. 6,667,792).

Regarding claim 1, Kwak discloses a digital DLL apparatus for use in semiconductor memory device operating in synchronization with an external clock, comprising: a frequency-detecting unit (figure 3, direct phase detector 350) that receives the external clock (ext_clk), detects clock frequency information of the external clock, and outputs the detected clock frequency information (detector 350 outputting the detected clock frequency information to the delay line unit 320); and a duty cycle correction circuit that corrects the duty cycle of the external clock in response to the clock frequency information (Figure 3, delay line unit 320 incorporated with blend circuit 330 correcting the frequency of the external clock to synchronize with internal clock based on the detecting signal; col. 5, lines 29+).

Regarding claim 2, Kwak discloses the digital DLL apparatus for use in semiconductor memory device having all of the limitation of claim 1, wherein the duty cycle correction circuit comprises: a first delay locked loop that receives the external clock, inverts and delays the external clock, synchronizes the delayed external clock with the inverted external clock, and outputs the delayed synchronized external clock (figure 3, third delay line 323 receives the external clock (ext_clk), inverted and delay the external clock, synchronizes the delayed external clock with the inverted external clock, and output the delayed synchronous external clock); a second delay locked loop that receives and delays the inverted external clock, synchronizes the delayed inverted external clock with the external clock, and outputs the delayed synchronized inverted clock (figure 3, fourth delay line 326 receives the external clock (ext_clk), inverted and delay the external clock, synchronizes the delayed external clock with the inverted external clock, and output the delayed synchronous external clock); and an interpolation circuit which interpolates a signal inverting the output signal of the first delay locked loop with the output signal of the second delay locked loop, and outputs the interpolated signal (figure 3, blend circuit 330 blending the first and second signal and outputting the blended signal is same as claimed interpolating the signals of delay circuit and outputting the output signal; col. 6, lines 33+).

Regarding claims 3-4, Kwak discloses the digital DLL apparatus for use in semiconductor memory device of claim 2, wherein the interpolation circuit comprises: a first inverting circuit that receives the signal inverting the output signal of the first delay locked loop, inverts the received signal, and outputs the inverted signal (figure 8, first clock processing circuit 820 inverting the received signal and output the inverted signal); a second inverting circuit that inverts the output signal of the second delay locked loop and outputs the inverted signal, the

output end of the first inverting circuit and the output end of the second inverting circuit connected with each other (figure 8, second clock processing circuit 830 inverting the received signal and output the inverted signal); a third inverting circuit that receives and inverts the output signal of the first inverting circuit and the output signal of the second inverting circuit, and outputs the inverted signal (figure 8, inverter 840 receives and inverts the output signal of the first and second processing circuit); and a plurality of capacitors having predetermined capacitances, connected between a ground power supply and respective input ends of the first, second, and third inverting circuits, wherein the capacitances of the plurality of capacitors are controlled by the clock frequency information; wherein when the clock frequency of the external clock is high, the capacitances of the plurality of capacitors are small, and when the clock frequency of the external clock is low, the capacitances of the plurality of capacitors are large (does not shown, but inherently, capacitors resistors or transistors should be in the circuit such as to store and delaying the clock signal (charges) that representing the clock information for the circuit and the charges that storing by the capacitors would have the similar functionality as claimed).

Regarding claim 5, Kwak discloses the digital DLL The semiconductor memory device of claim 1, wherein the frequency detecting unit comprises: a frequency detecting circuit (figure 3, detector 350) that receives the external clock and detects the clock frequency of the external clock; an analog-to-digital converter (ADC) that receives an output signal of the frequency detecting circuit, converts the output signal into a digital signal, and outputs the digital signal (figure 3, controller 321 receives the output signal of the frequency detector 350, output the control signal in digital form, converting the analog signal into digital form within the control

circuit); and a register that receives the output signal of the ADC and stores the output signal of the ADC as the clock frequency information (figure 3, shift register 323 receives the output signal of the controller 321 as the clock frequency information).

Claims 6-8, 9-11 and 12-15 claiming the similar limitation as previously discussed in claims 1-5. Therefore, they are analyzed as previously discussed with respect to claims 1-5.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
November 03, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818